

NORMAL MODE
GENERAL PURPOSE
REGISTERS 100

R0
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15

R8
R9
R10
R11
R12
R13
R14
R15

INTERRUPT MODE
BANKED REGISTERS
102

FIG. 1
(PRIOR ART)

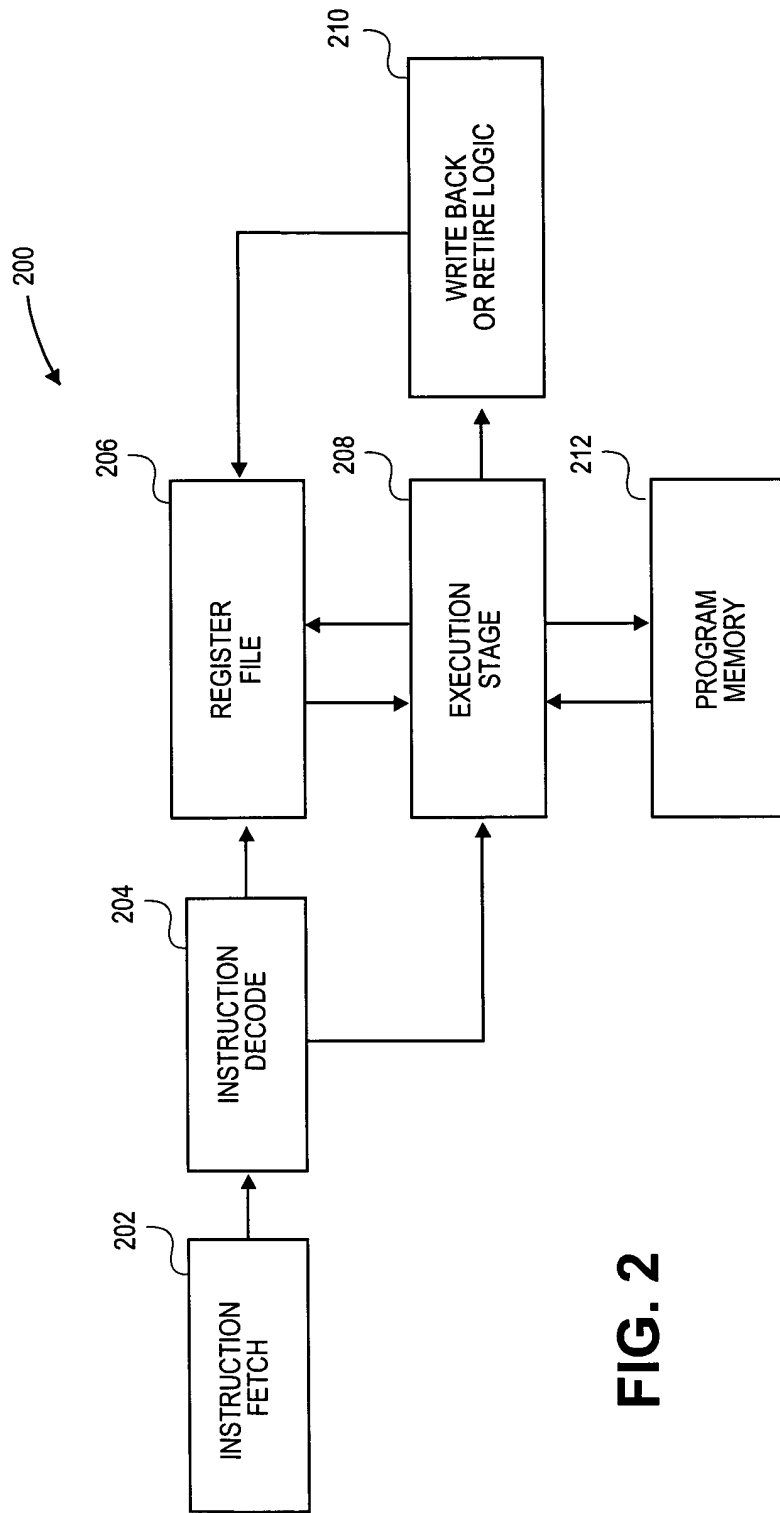


FIG. 2

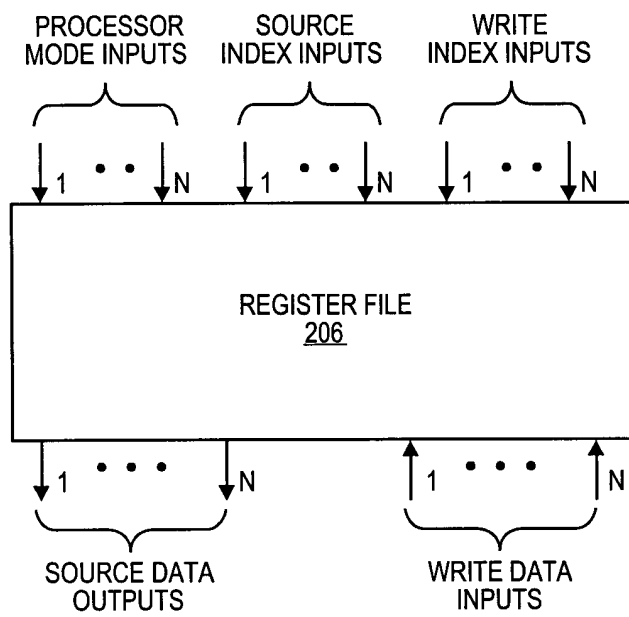


FIG. 3

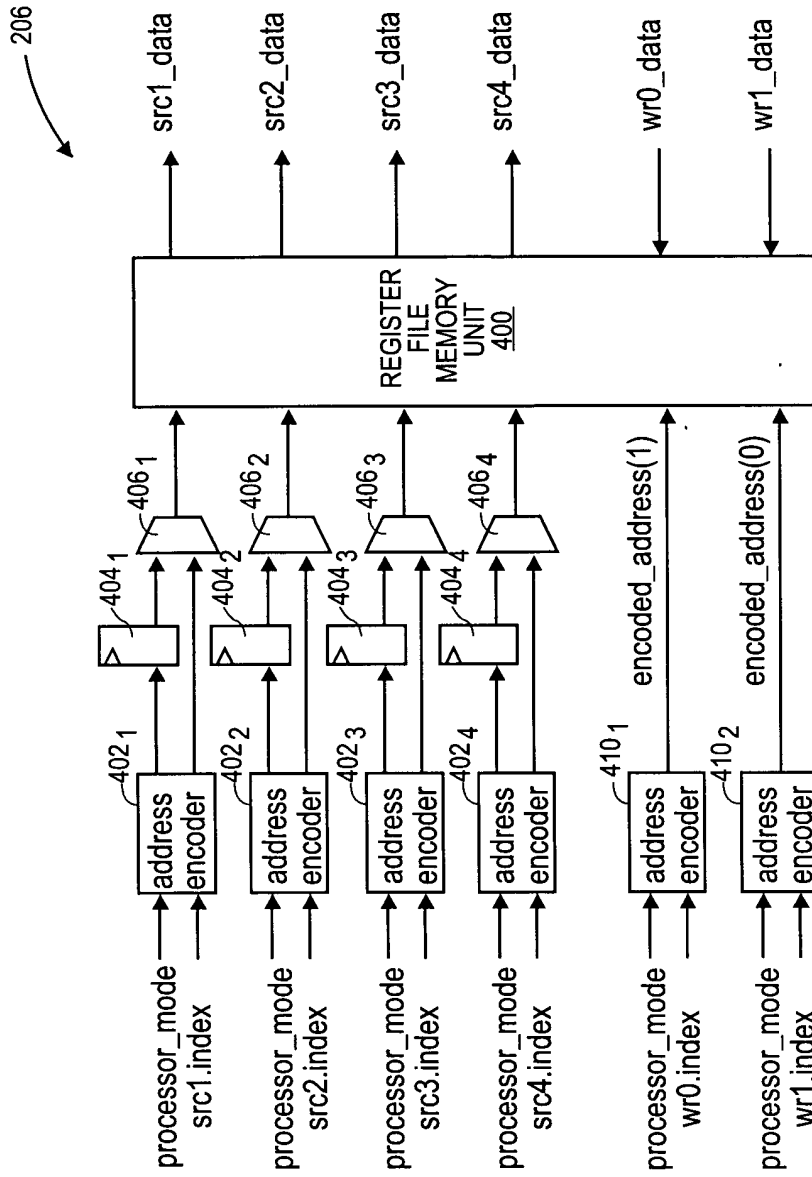


FIG. 4

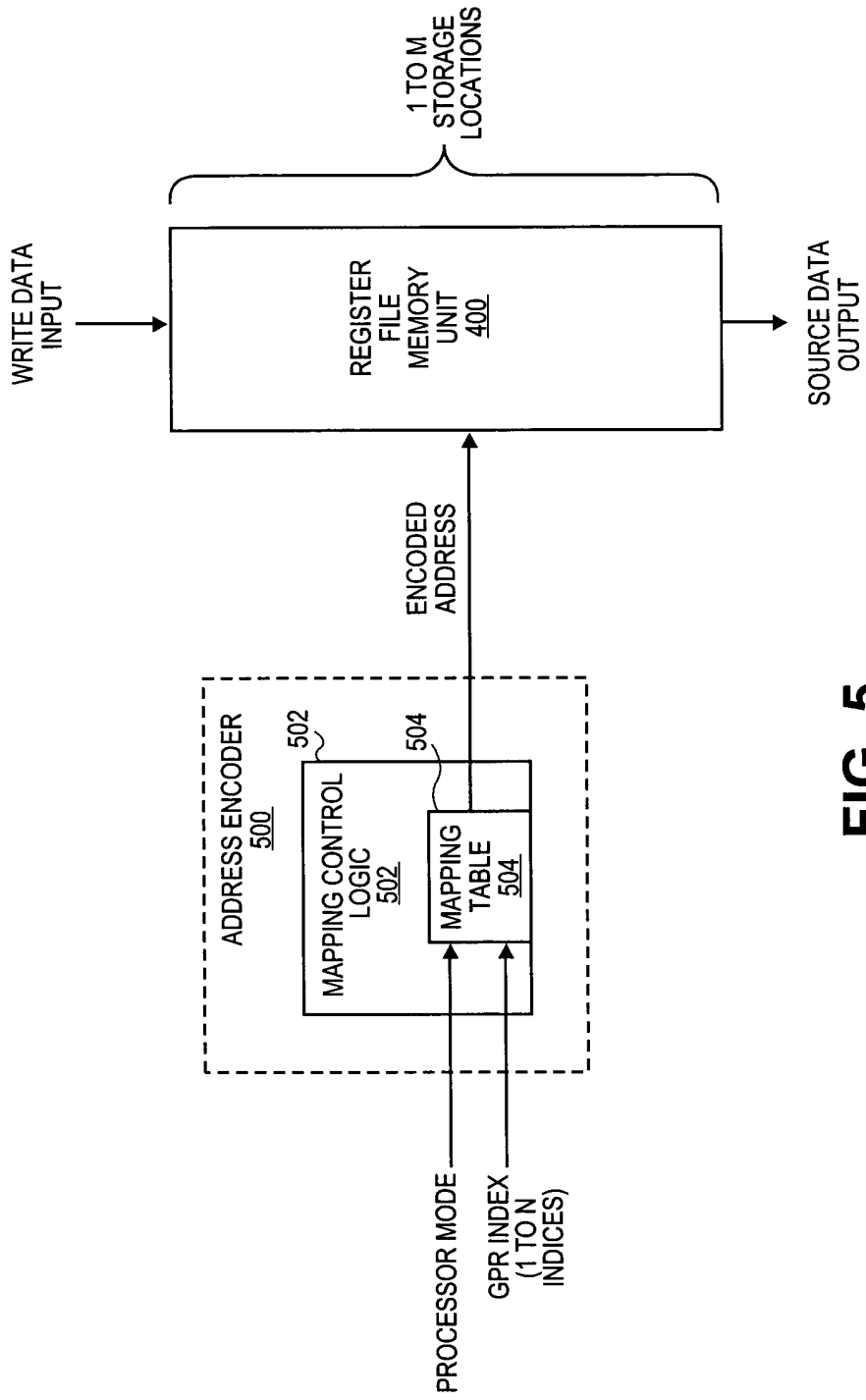


FIG. 5

GENERAL PURPOSE
REGISTER (GPR)
INDICES
600

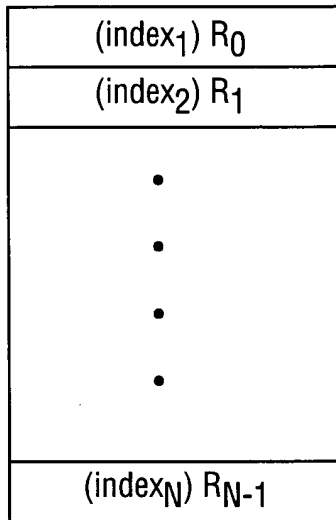


FIG. 6

MAPPING
TABLE
504

GPR INDICES	PROCESSOR MODE	ENCODED ADDRESS
$Index_1$ ● ● $Index_N$	Mode 1 - Mode K	ENCODED ADDRESS ₁
$Index_1$ ● ● $Index_N$	Mode 1 - Mode K	●
		●
		●
		●
$Index_1$ ● ● $Index_N$	Mode 1 - Mode K	ENCODED ADDRESS _M

FIG. 7

GENERAL PURPOSE
REGISTER (GPR) INDICES
800

(0000) R ₀
(0001) R ₁
(0010) R ₂
(0011) R ₃
(0100) R ₄
(0101) R ₅
(0110) R ₆
(0111) R ₇
(1000) R ₈
(1001) R ₉
(1010) R ₁₀
(1011) R ₁₁
(1100) R ₁₂
(1101) R ₁₃
(1110) R ₁₄
(1111) R ₁₅

FIG. 8

MAPPING TABLE

904

GPR Indices (Registers)	Processor Mode	Encoded Address (memory location)
(0000) R ₀ (0001) R ₁ (0010) R ₂ (0011) R ₃ (0100) R ₄ (0101) R ₅ (0110) R ₆ (0111) R ₇	MODES 1-N	00000 00001 00010 00011 00100 00101 00110 00111
(1000) R ₈ (1001) R ₉ (1010) R ₁₀ (1011) R ₁₁ (1100) R ₁₂	MODE 1	01000 01001 01010 01011 01100
(1101) R ₈ (1110) R ₉ (1111) R ₁₀ (1110) R ₁₁ (1100) R ₁₂	MODE 2	01101 01110 01111 10000 10001
(1100) R ₁₅ (1110) R ₁₄ (1100) R ₁₃	MODE 3	10011 10010 10011
(1110) R ₁₄ (1100) R ₁₃	MODE 4	10100 10101
(1110) R ₁₄ (1100) R ₁₃	MODE 5	10110 10111
(1000) R ₈ (1001) R ₉ (1010) R ₁₀ (1011) R ₁₁ (1100) R ₁₂ (1101) R ₁₃ (1110) R ₁₄ (1111) R ₁₅	MODE N	11000 11001 11010 11011 11100 11101 11110 11111

FIG. 9

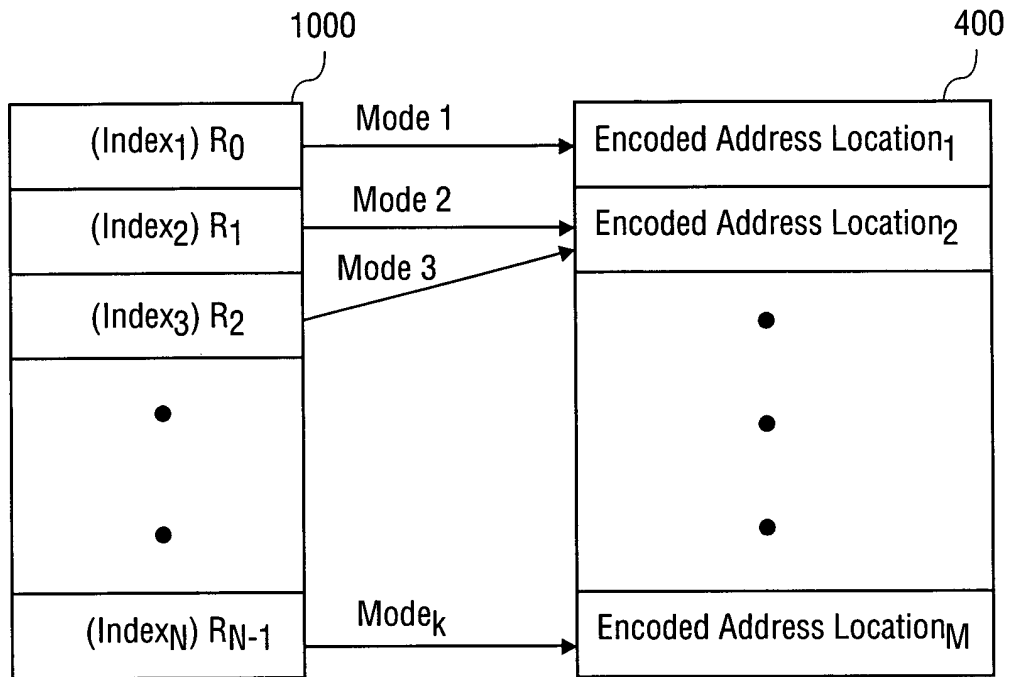


FIG. 10A

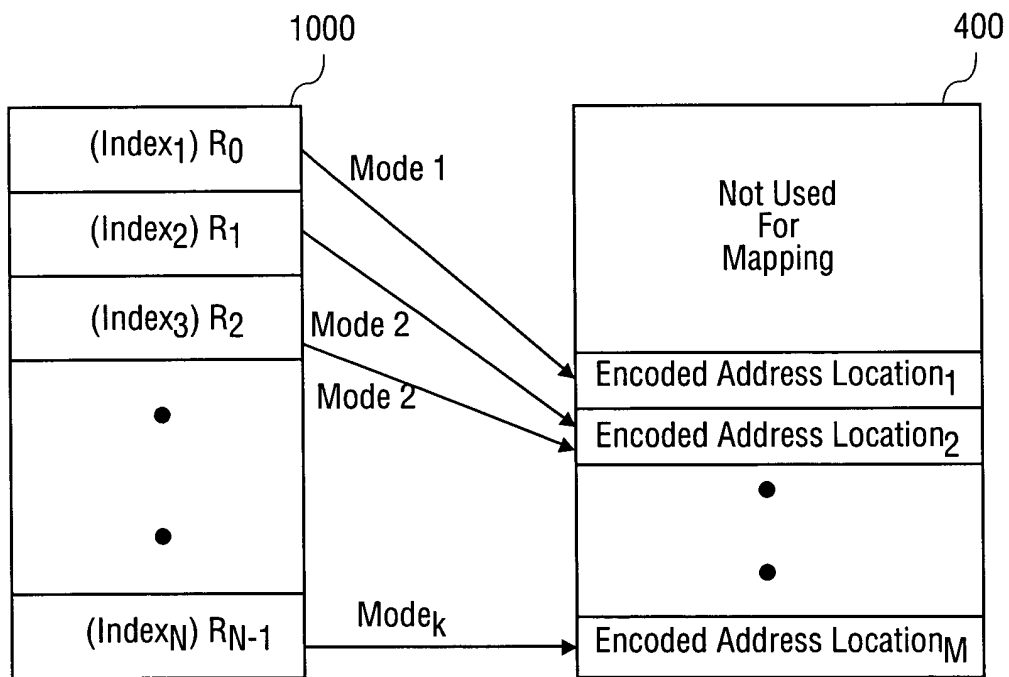


FIG. 10B

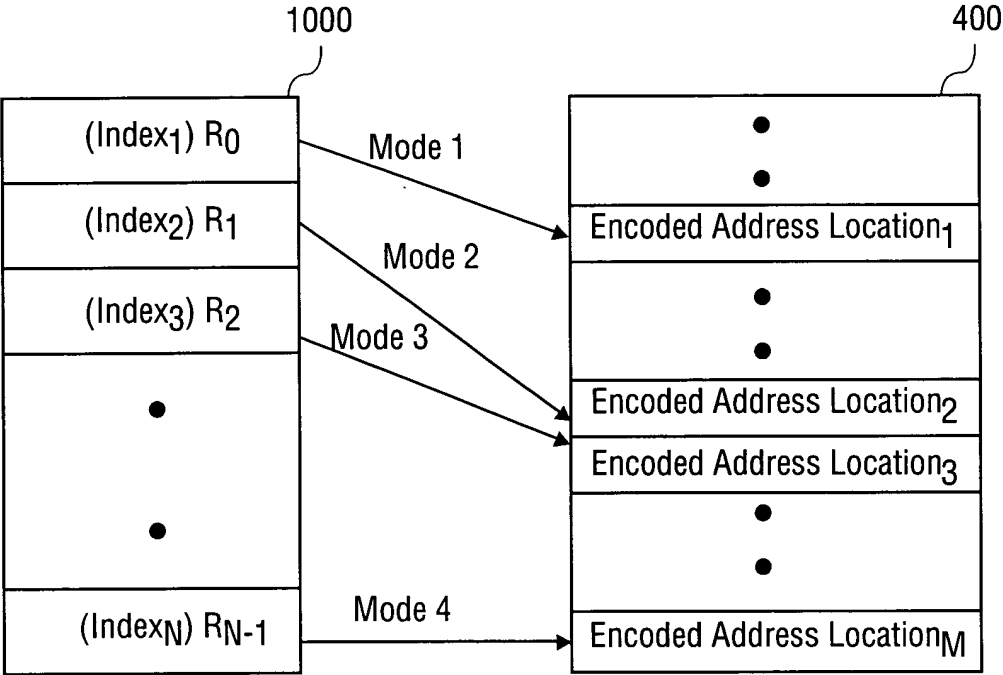


FIG. 10C

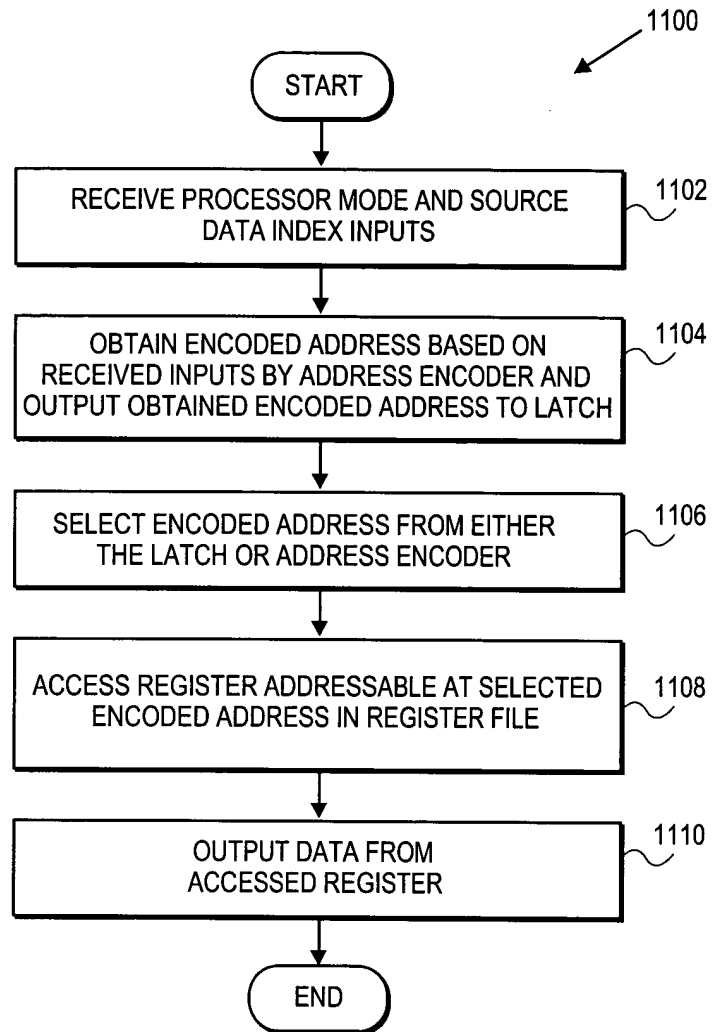


FIG. 11

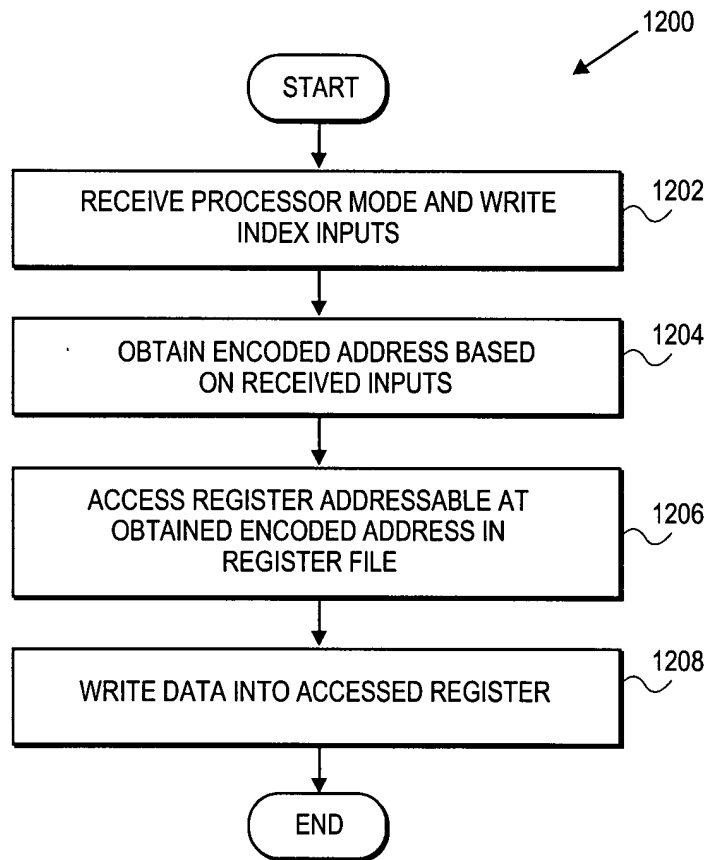


FIG. 12